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AGILENT TECHNOLOGIES, INC.
INTELLECTUAL PROPERTY ADMINISTRATION, LEGAL DEPT.
P.O. BOX 7599
M/S DL429
LOVELAND, CO 80537-0599

EXAMINER	
SHRADER, LAWRENCE J	

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 09/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/659,256	KRECH ET AL.	
	Examiner	Art Unit	
	Lawrence Shrader	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the amendment filed on 05/17/2004.

2. The arguments set forth in the Applicant's amendment have been fully considered, but are not persuasive. Claims 1 – 18 remain rejected.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 3 – 5, and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Kamiyama et al., U.S. Patent 5,991,868 (hereinafter referred to as Kamiyama).

In regard to claim 1:

Kamiyama discloses an apparatus for conditional branching comprising:

> *"a sequencer executing a plurality of program instructions, one or more of said program instructions including a conditional branch instruction, said conditional branch instruction specifying a branch condition address and a conditional instruction,"*

Kamiyama discloses a sequence of instructions (inherent in an instruction based architecture) including a conditional branch (Figure 6), a branch unit (Figure 6, item 107) that

selects flags read out of a memory, then that flag is used to determine a branch condition (column 6, lines 49 – 67).

> *"a branch unit comprising a flag selection memory capable of being programmed with a plurality of selection values, each selection value providing independent selection input into a respective plurality of first flag selectors, each respective first flag selector presenting at an output a respective first stage selected flag from a plurality of available flags based upon each said selection value, a second flag selector accepting a plurality of said first stage selected flags and selecting one of said first stage selected flags to present as a branch flag based upon said branch condition address, said branch flag indicating to said sequencer whether to branch according to said conditional instruction."*

Kamiyama discloses a branch unit (Figure 6) comprising a flag selection memory programmed with a plurality of values (see ref. 106) wherein each value provides an independent input to the flag selector (see inputs at ref. 107); each respective first flag selector in ref. 107 presents an output from a plurality of flags based on the flag group designation (column 4, lines 39 – 47; see Figure 6, ref, 6-1 through 6-4); a second flag selector accepting the plurality of flags and (judging unit accepting input from the flag selection unit; Figure 6, judging unit; column 4, lines 48 – 56) selecting one as a branch flag based upon a branch condition address (see Figure 7 B; column 5, lines 35 – 49). A determination to branch or not is then resolved.

In regard to claim 3, incorporating the rejection of claim 1:

> *"...said flag selection memory comprising a plurality of programmable registers."*

Kamiyama discloses a program status word, composed of 2 flag groups (multiple registers, see Figure 6 and column5, lines 19 – 33).

In regard to claims 4 and 5, incorporating the rejection of claim 1:

> *"...each said first flag selectors comprising a multiple input, single output multiplexer."*

"...said second flag selector comprising a multiple input single out multiplexer."

Kamiyama discloses first flag selectors comprising a multiple input and single output multiplexer (e.g., Figure 6 flag groups 6-1 to 6-4 selecting one out of two); and a second flag selector comprising a multiple input and single out multiplexer (e.g., Figure 6 judging unit selecting one out of four).

In regard to claim 7, incorporating the rejection of claim 1:

"... wherein said branch address comprises a plurality of bits in said conditional branch instruction."

Kamiyama discloses a branch address comprising a plurality of bits in a conditional branch instruction (e.g., Figure 7B).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiyama et al., U.S. Patent 5,991,868 in view of Asakawa et al., U.S. Patent 5,408,620 (hereinafter referred to as Asakawa).

In regard to claim 2, incorporating the rejection of claim 1:

"...further comprising a plurality of said branch units and further comprising an operator that accepts a respective plurality of said branch flags and logically combines said

branch flags to create a branching bit, said branching bit indicating whether said sequencer is to branch according to said conditional instruction."

Kamiyama teaches a sequence of instructions (inherent in an instruction based architecture) including a conditional branch (Figure 6), a branch unit (Figure 6, item 107) that selects flags read out of a memory, then that flag is used to determine a branch condition (column 6, lines 49 – 67), but Kamiyama does not teach a plurality of branch instruction units comprising an operator logically combining branch flags to create a branch bit. Asakawa, however, teaches multiple branch instruction units (column 2, lines 50 – 56), and a circuit for processing conditional branching instructions that uses a multiple input logical AND as an operator (column 5, line 49 to column 6, line 54; Figure 7, item 132). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to modify the conditional branch teaching of the Kamiyama invention with the teaching of Asakawa to operate multiple branching units, and to provide an operator accepting multiple flags and logically combining, because the modification enhances the Kamiyama invention to produce a branching bit indicating a certain condition to by resolving multiple branch conditions in deciding whether or not to branch as taught by Asakawa (Abstract)

In regard to claim 6, incorporating the rejection of claim 2:

"...said operator comprising a multiple input logical AND operator."

Kamiyama teaches a sequence of instructions (inherent in an instruction based architecture) including a conditional branch (Figure 6), a branch unit (Figure 6, item 107) that selects flags read out of a memory, then that flag is used to determine a branch condition (column 6, lines 49 – 67), but Kamiyama does not explicitly reference a multiple input logical

AND operator. However, Asakawa discloses the branch selection logic that contains an AND operator to select from the multiple branch units (Asakawa: Figure 7, item 132). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the conditional branch teaching of the Kamiyama invention with the teaching of Asakawa to operate multiple branching units, and to provide an operator accepting multiple flags and logically combining with AND logic, because the combination enhances the Kamiyama invention to produce a branching bit indicating a certain condition to by resolving multiple branch conditions in deciding whether or not to branch as taught by Asakawa (Abstract)

7. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiyama et al., U.S. Patent 5,991,868 in view of Khim Yeoh e et al., U.S. Patent 5,274,770 (hereinafter referred to as Khim).

In regard to claim 8, incorporating the rejection of claim 1:

> *"...further comprising a b1not0 bit in said conditional branch instruction directing said sequencer whether it is to branch on a one or a zero of said branch flag."*

Kamiyama discloses a conditional branch instruction, but does not disclose a direction to the sequencer whether it is to branch on a one or a zero. However, Khim discloses that execution of an instruction can be modified by a bit in a flag register wherein the instruction branches on the condition represented by a register (column 2, lines 9 – 14). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the branch judging teaching of the Kamiyama invention with the teaching of Khim, because the combination provides the Kamiyama invention with the means to direct the sequencer to a

branch/no branch on a condition specified by a bit representation as taught by Khim allowing greater control over the branching function.

8. Claims 9 – 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiyama et al., U.S. Patent 5,991,868 in view of Asakawa et al., U.S. Patent 5,408,620 (hereinafter referred to as Asakawa), and further in view of Khim Yeoh e et al., U.S. Patent 5,274,770 (hereinafter referred to as Khim).

In regard to claim 9, incorporating the rejection of claim 2:

> *"... further comprising a b1not0 bit in said conditional branch instruction directing said sequencer whether it is to branch on a one or a zero of said branch flag."*

Kamiyama teaches a sequence of instructions (inherent in an instruction based architecture) including a conditional branch (Figure 6), a branch unit (Figure 6, item 107) that selects flags read out of a memory, then that flag is used to determine a branch condition (column 6, lines 49 – 67), but neither Kamiyama nor Asakawa teaches a direction to the sequencer whether it is to branch on a one or a zero. However, Khim discloses that execution of an instruction can be modified by a bit in a flag register wherein the instruction branches on the condition represented by a register (column 2, lines 9 – 14). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the branch judging as taught by Kamiyama with the teaching of Asakawa operating multiple branching units, and to provide an operator accepting multiple flags and logically combining then, modified with Khim, because the combination provides the Kamiyama/Asakawa combination with the

means to direct the sequencer to a branch/no branch on a condition specified by a bit representation as taught by Khim allowing greater control over the branching function.

In regard to claim 10, incorporating the rejection of claim 9; and

In regard to claim 11, incorporating the rejection of claim 10:

> *"...further comprising a dual input selector accepting said branching bit and an inverse of said branching bit, said b1not0 bit operating on said dual input selector."*
>
> *"...wherein said dual input selector is a dual input single output multiplexer."*

In reference to claims 10 and 11, official notice is taken that a dual input, single output selector/multiplexer is well known in the art with inputs arranged in various configurations.

9. Claims 15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiyama et al., U.S. Patent 5,991,868 in view of Ochiai et al., U.S. Patent 4,742,466 (hereinafter referred to as Ochiai).

In regard to claim 15:

> *"a compiler for converting source code including one or more conditional branch instructions into object code, the compiler assigning values for a branch condition address and values for a flag selection memory,"*

Kamiyama teaches a sequencer and a conditional branching unit for executing program instructions. Although compiling is not explicitly addressed in the invention, source code is inherently compiled in the Kamiyama invention in order to be executed. However, Ochiai teaches a compiler that converts source code including conditional branch instructions including an address and a flag (column 2, line 63 to column 3, line 12). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the compiler as

taught by Ochiai with the sequencer and branching unit as taught by Kamiyama in order to create the object code that is processed in the sequencing and conditional branching system.

> *"a sequencer executing said object code comprising one or more of said conditional branch instructions, each said conditional branch instruction specifying a branch condition address and a conditional instruction,"*

Kamiyama discloses a sequence of instructions (inherent in an instruction based architecture) including a conditional branch (Figure 6), a branch unit (Figure 6, item 107) that selects flags read out of a memory, then that flag is used to determine a branch condition (column 6, lines 49 – 67).

> *"a branch unit comprising said flag selection memory capable of being programmed with a plurality of selection values, each selection value providing independent selection input into a respective plurality of first flag selectors, each respective first flag selector presenting at an output a respective first stage selected flag from a plurality of available flags based upon each said selection value, a second flag selector accepting a plurality of said first stage selected flags and selecting one of said first stage selected flags to present as a branch flag based upon said branch condition address, said branch flag indicating to said sequencer whether to branch according to said conditional instruction."*

Kamiyama discloses a branch unit (Figure 6) comprising a flag selection memory programmed with a plurality of values (see ref. 106) wherein each value provides an independent input to the flag selector (see inputs at ref. 107); each respective first flag selector in ref. 107 presents an output from a plurality of flags based on the flag group designation (column 4, lines 39 – 47; see Figure 6, ref, 6-1 through 6-4); a second flag selector accepting the plurality of flags and (judging unit accepting input from the flag selection unit; Figure 6, judging unit; column 4, lines 48 – 56) selecting one as a branch flag based upon a branch condition address (see Figure 7 B; column 5, lines 35 – 49). A determination to branch or not is then resolved.

In regard to claim 18, incorporating the rejection of claim 15:

"...further comprising one or more arithmetic logic units that supply said plurality of available flags."

Kamiyama discloses a 16-bit calculator that supplies the plurality of flags (e.g., see Figure 6.

10. Claims 12 – 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogata et al., U.S. Patent 6,546,550 (hereinafter referred to as Ogata) in view of Kamiyama et al., U.S. Patent 5,991,868.

In regard to claim 12:

A method for compiling source code containing one or more conditional branching instructions comprising the steps of:

"interpreting the source code, the source code comprising a plurality of program instructions,

identifying each conditional branch instruction in said source code, and for each conditional branch instruction, determining a set of flags as a subset of all available flags upon which each said conditional branch instruction is based, identifying a flag selection value for each flag in said set of flags, and storing each said flag selection value to a to a respective one of two or more flag selection register array elements, assigning a branch condition address for said conditional branching instruction, encoding said branch condition address in a binary representation of said conditional branching instruction, and storing said encoded one or more conditional branching instructions and said flag selection register array elements in an object code format."

Ogata teaches an interpreter that converts source code (Abstract) and identifies each conditional branch condition in the source code (See Figure 1, S1), and a JIT compiler transforming the JAVA byte codes into machine (object) code (e.g., Figure 2), but does not teach a determining a set of flags upon which a conditional branching is based. However, Kamiyama

discloses a branch unit (Figure 6) determining a set of flags being a subset of all available flags upon which a branch is based (see ref. 106); identifying a flag selection value for each flag the set (ref. 106 and 107); storing the flag values in a respective one of two or more of array elements (see Figure 6, ref, 6-1 through 6-4); assigning a branch condition address for the said conditional branch instruction (e.g., Figure 4B), but does not disclose encoding the branch condition address in a binary representation and storing the conditional branch instructions in an object format, although the decoding of the instructions in Kamiyama (e.g., see Figure 6) implies that the code has been compiled into object code. Therefore it would have been obvious to one skilled in the art at the time the invention was made to combine interpreter with the encoding of branch instructions into object code as taught by Ogata the sequencer and branching unit as taught by Kamiyama because combination provides the Ogata invention with a means to conduct a flag selector mechanism in order to determine a branch flag based upon the branch condition address allowing the branch to be taken based on a selected flag group as taught by Kamiyama (Abstract).

In regard to claim 13, incorporating the rejection of claim 12:

> *"...further comprising the step of re-ordering said set of flags to a set placement format."*

Kamiyama discloses a program status word 106 for storing flag groups to be changed (re-ordered) in accordance with the calculation results of the calculator (column 4, lines 1 – 12).

11. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ogata et al., U.S. Patent 6,546,550 (hereinafter referred to as Ogata) in view of Grady et al., U.S. Patent 5,276,776 (hereinafter referred to as Grady).

In regard to claim 14, incorporating the rejection of claim 12:

> *"...further comprising the step of converting all disjunctive operations to a conjunctive equivalent."*

Ogata teaches an interpreter that converts source code (Abstract) and identifies each conditional branch condition in the source code (See Figure 1, S1), and a JIT compiler transforming the JAVA byte codes into machine (object) code (e.g., Figure 2), but does not teach converting all disjunctive operations to a conjunctive equivalent. However, Grady teaches a system that accepts disjunctive rules and converts them to conjunctive equivalent (column 7, lines 7 – 20). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine interpreter/compiler of Ogata with the teaching of Grady because the combination allows the compiler to convert disjunctive logical operations specified in said conditional branch instructions to an equivalent conjunctive logical operation where the conditions might be "ANDed" together.

12. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiyama et al., U.S. Patent 5,991,868 in view of Ochiai et al., U.S. Patent 4,742,466 as applied to claim 15 above, and further in view of Grady et al., U.S. Patent 5,276,776.

In regard to claim 16, incorporating the rejection of claim 15:

> *"...said compiler also converting disjunctive logical operations specified in each said conditional branch instructions to an equivalent conjunctive logical operation."*

Kamiyama teaches a sequencer and a conditional branching unit for executing program instructions, but neither Kamiyama nor Ochiai teaches the conversion of all disjunctive operations to a conjunctive equivalent. However, Grady teaches a system that accepts

disjunctive rules and converts them to conjunctive equivalent (column 7, lines 7 – 20). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine the flag and conditional branch instruction processing of Kamiyama with the compiling of conditional branch instruction carrying the branch address as taught by Ochiai and further modifying it with the teaching of Grady because the combination provides the compiler the means to converts disjunctive logical operations specified in said conditional branch instructions to an equivalent conjunctive logical operation where the conditions might be "ANDed" together.

13. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiyama et al., U.S. Patent 5,991,868 in view of Ochiai et al., U.S. Patent 4,742,466, and further in view of Grady et al., U.S. Patent 5,276,776 as applied to claim 16 above, and further in view of Prasanna, U.S. Patent 6,272,599.

In regard to claim 17, incorporating the rejection of claim 16:

> *"...said compiler setting a b1notO bit for said program instruction if said logical operation is converted from said disjunctive logical operation to said equivalent conjunctive logical operation."*

Kamiyama, Ochiai and Grady combine to teach a compiler to process conditional branch instructions, a sequence of instructions executed as object code, and a branch unit to determine whether to take a branch or not. None teach the compiler setting bits on a certain condition. However, Prasanna teaches a compiler capable of selectively setting bits based on a certain condition. (column 2, lines 1 – 8, 49 – 54). Therefore, it would have been obvious to one skilled in the art at the time the invention was made to combine Kamiyama, Ochiai and Grady so that

the executable code might be compiled and executed by the sequencer and branching unit with equivalent conjuntive logic (incorporated from claim 16) based on a signal flag set by the compiler as further taught by Prasanna.

Response to Arguments

14. Applicant's arguments filed on 5/17/2004 have been fully considered but they are not persuasive:

The Applicant has argued:

"...claim 1 is amended to clarify the programmable and independent selection memory wherein it is "capable of being programmed with plurality programmable selection values, each selection value providing independent selection input into a respective plurality of first flag selectors, each respective first flag selector presenting at an output respective first stage selected flag from a plurality of available flags based upon each said selection value". Support for the amendment found on page 21, line 17 through page 22, line 5 of the Specification and FIGURE 5 of the drawings. The Kamiyama patent does not teach a "flag selection memory" ... "programmed with a plurality of selection values, each selection value providing independent selection input into a respective plurality of first flag selectors" for "presenting" ... "a first stage selected flag from a plurality of available flags based upon each said selection value". Accordingly, claim 1 as amended believed be patentably distinct from teachings the Kamiyama patent and allowance is solicited."

Examiner's response:

The amended language of claim 1 has been considered, but, as indicated in the office action above, Kamiyama still reads on the claim as amended. The claimed invention is described in terms of a multi stage selection of a branch flag with intermediate programming of values in selectors, which is precisely what the Kamiyama invention entails. Kamiyama teaches a flag selection memory at ref 106 in Fig. 6. The indicated "psw" is clearly a memory structure

containing a plurality of selection values eventually determined in the selection stages of memory gates 6-1 through 6-4 and the condition judging unit (both in ref 107 of Fig. 6).

The argument concerning independent claims 12 and 15 are similar since the subject matter is substantially the same.

Conclusion

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence Shrader whose telephone number is (703) 305-8046. The examiner can normally be reached on M-F 08:00-16:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lawrence Shrader
Examiner
Art Unit 2124

30 August 2004

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100